# JNIT JAGANNATH GUPTA INSTITUTE OF ENGINEERING & TECHNOLOGY JAIPUR I-Mid Term Examination Session 2017-2018 B.Tech .3<sup>rd</sup>. Year .6<sup>th</sup>. Semester Branch: ECE Subject: Control System Engg

Time: 10:00 am-11:30am Date: 16/02/2018 Subject: Control System Engg Subject Code:6EC5A Max. Marks: 20

#### Attempt any four questions out of following five questions. All Que carry equal marks.

Q.1 What is control system? Write difference between open loop & Close loop Control system with Example and Diagram.

Syste.	in with Example and Diagram.	
ANS		
1.5	Control System	
connected is an esse the syster to obtain necting be engineerin by the fui and its av regulate th	I system comprises of control element (subsystem) and plant (system) which a d together for the purpose of controlling the response of the system. So, cont ential part of the system and helps in obtaining the specified value of output fn m. On the other hand control is that part of system which enables the syst the desired response. Combining both of them (control and system) and c etween input and output is called control system and study of control system ag field is termed as Control System Engineering. For example, heat produ mace depends on the flow of fuel. In this system, subsystem called fuel va- ctuators move by which heat outputs from the furnace can be controlled the room temperature. Figure 1.2 shows the simplest form of control system an output or response for a given input or excitation.	rol om on- i in ced ulve l to
	Input (Excitation)	
	Figure 1.2 : Block diagram of a control system	
For example a highway	ple, assume an automobile speed control system as shown in figure 1.3 i y where the speed limit is $65 \text{ km/hr}$ . The driver's control system acts as foll	s on ows:
1. Actua	al speed is detected by the eye that observes the speedometer.	
2. The b	brain assesses this speed in comparison with the desired speed.	
accelerator break.	in judges the speed is too fast, it directs the foot to ease up on the and the speed is too slow then it direct the foot to make pressure on converged by the nerves in accordance to achive desired speed.	
Besired + ↓ -	$\begin{array}{c} \text{Brain} \longrightarrow \text{Legs} \longrightarrow \text{Accelerometer} \longrightarrow \text{Vehicles} \longrightarrow \\ \text{Output} \\ \text{speed} \\ \hline \\ \text{Speedometer} \end{array}$	

Figure 1.3 : Block diagram of automobile speed control system

# Differences Between Open Loop Control System and Closed-Loop Control System

S.No.	Open Loop Control Systems	Closed Loop Control Systems
1.	In open loop systems, the control action is independent of the output.	In closed loop systems, control action is dependent on the output.
2.	They are sensitive to external disturbances and internal variations in system parameters	They are very less sensitive to external disturbances and internal variations in system parameters.
3.	There is a need to use accurate as well as expensive components to obtain the accurate control of given plant.	We can even use less accurate as well as in-expensive components to obtain accurate control of given plant.
4.	It is used only where inputs to the system are known ahead of time.	It can be used when inputs are not known ahead of time.
5.	Number of components used in this system are less. So they are simple and cheap.	Number of components used in these system are more. So they are complex and costly.

#### able 1.1 : Difference Between Open Loop and Closed Loop Control Systems

## Q.2 ANS Explain Force-Voltage Analogy.



# Force-Voltage Analogy and Torque-Voltage Analogy:

Consider a series R-L-C circuit as shown in figure 2.9.

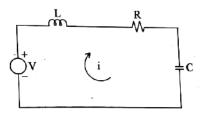


Figure 2.9 Series R-L-C circuit

Applying Kirchoff's voltage law.

$$V = Ri + L\frac{di}{dt} + \frac{1}{C}\int idt$$

In terms of charge, equation becomes [i.e. i = dq/dt]

$$V = R \frac{dq}{dt} + L \frac{d^2q}{dt^2} + \frac{1}{C}q \qquad \dots \dots (2.3)$$

-ma

Now, consider a mechanical system as shown in figure 2.7 and for that system equation of motion is given by equation (2.1) as under

$$F = M\frac{d^2x}{dt^2} + B\frac{dx}{dt} + Kx$$

If we compare a mechanical translational system with an electrical series circuit  $g_{i\nu e_{II}}$ by equation (2.3) we find similarity between them. They are therefore called analogous systems or we can say that behaviour of the mechanical system shown in figure 2.7 can be completely determined by simple R-L-C electrical circuit of figure 2.9 by making appropriate conversions of physical quantities as listed in the table. Here the following analogies can be drawn :

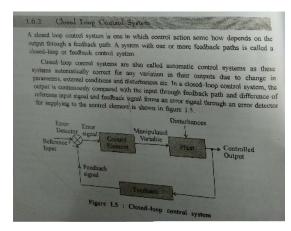
- 1. Applied force F is analogous to applied voltage V.
- 2. Mass M is analogous to inductance L. 3.
- Coefficient of viscous friction B is analogous to resistance R.
- 4. Spring constant K is analogous to reciprocal of capacitance  $\frac{1}{C}$ .

5. Displacement x is analogous to electric charge q.

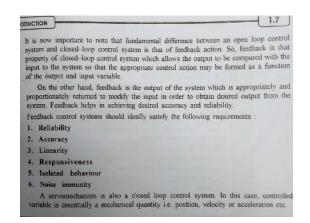
Similarly, if we compare a mechanical rotational system (figure 2.8) with an electrical series circuit (figure 2.9), we also find analogy between them. Both the analogies are

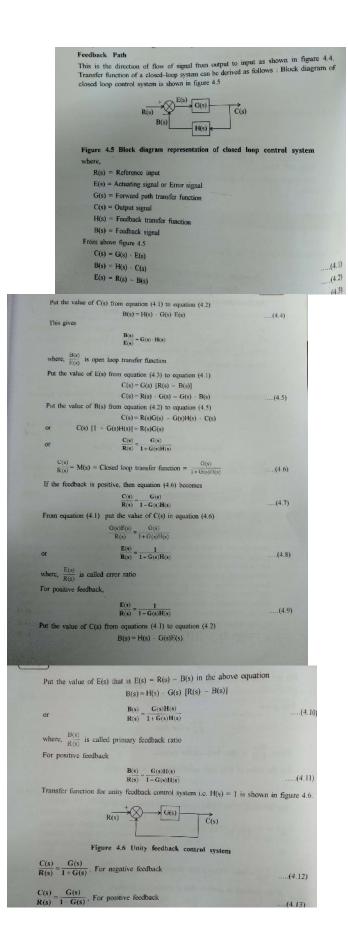
T-11 - 4 -		both the a
Table 2.2 Fo	rce voltage analogy and Torq	ue voltage of l
Detail	fechanical System	
motion	Transintional Motion	Electrical System
Torque T	Force F	I Denes R.T.
Angular	velocity	circuit)
velocity on	telocity	Voltage V
Angular	Displace	current i
displacement q	Displacement x	ab
Moment of	Mass M	charge q
inertia J Damping		Terl
constant B0	Viscous frint	Inductance L
Torsional	Viscous friction coefficient or damping constant B	P
constant k	Spring constant B	Resistance R
stant k	Spring constant K	
		Capacitance 1/C

writes the advantage and disadvantage of close loop control system .Drive an expression Q.3 for close loop gain.

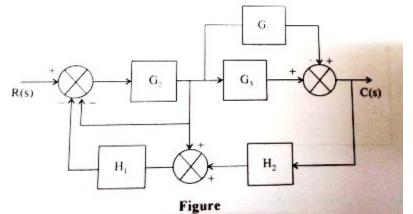


#### ANS

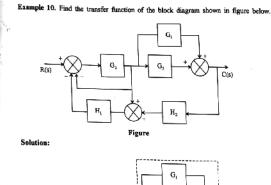


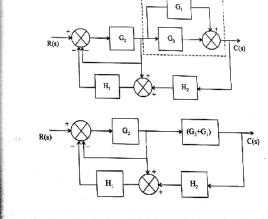


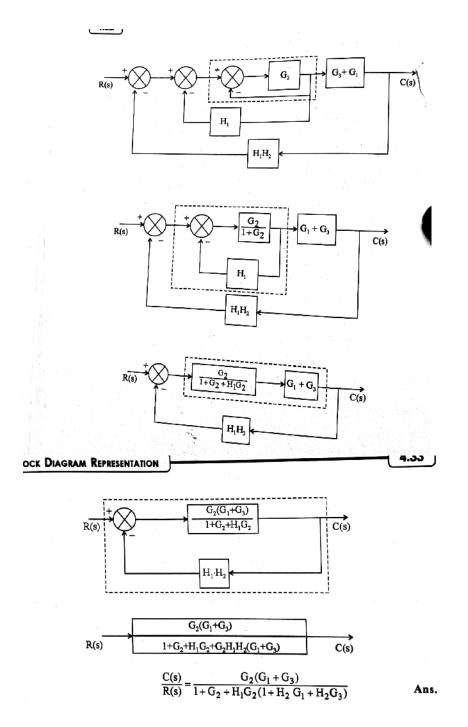
Q.4 Simplify the Block diagram given below and obtain the transfer function?



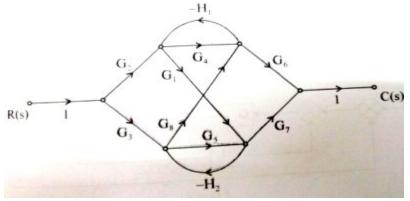








Q.5 The signal flow graph of a system is shown in figure .find the transfer function?



ANS

 $F_2 = G_3 G_5 G_7$  $F_3 = G_2 G_1 G_7$  $F_4 = G_3 G_8 G_6$  $F_5 = G_2 G_1 (-H_2) G_8 G_6 = - G_1 G_2 G_6 G_8 H_2$  $F_6 = G_3 G_8 (-H_1) G_1 G_7 = -G_1 G_3 G_7 G_8 H_1$ 

Individual loops

 $L_{11} = G_4(-H_1) = - G_4H_1$  $L_{12} = G_5(-H_2) = - G_5H_2$  $L_{13} = (-H_1)G_1(-H_2)G_8 = H_1H_2G_1G_8$ 

Two non-touching loops

 $NT_1 = (-G_4H_1)(-G_5H_2) = G_4G_5H_1H_2$ Forward path F<sub>1</sub> does not touch L<sub>12</sub> loop and forward path F<sub>2</sub> does not touch L<sub>11</sub> loop But all other paths touch both the loops. Therefore,

> $\Delta_1 = 1 + G_5 H_2, \quad \Delta_2 = 1 + G_4 H_1$  $\Delta_3 = \Delta_4 = \Delta_6 = 1$  $\Delta = 1 + G_4 H_1 + G_5 H_2 - H_1 H_2 G_1 G_8 + G_4 G_5 H_1 H_2$

 $\mathbf{T}.\mathbf{F} = \frac{G_2 G_4 G_6 (1 + G_5 H_2) + G_3 G_5 G_7 (1 + G_4 H_1) + G_2 G_1 G_7}{1 + G_4 H_1 + G_2 G_1 G_7}$  $1 + G_4H_1 + G_5H_2 - H_1H_2G_1G_8 + G_4G_5H_1H_2$ 

> $+\frac{G_3G_8G_6-G_1G_2G_6G_8H_2-G_1G_3G_7G_8H_1}{1+G_4H_1+G_5H_2-H_1H_2G_1G_8+G_4G_5H_1H_2}$ Ans.

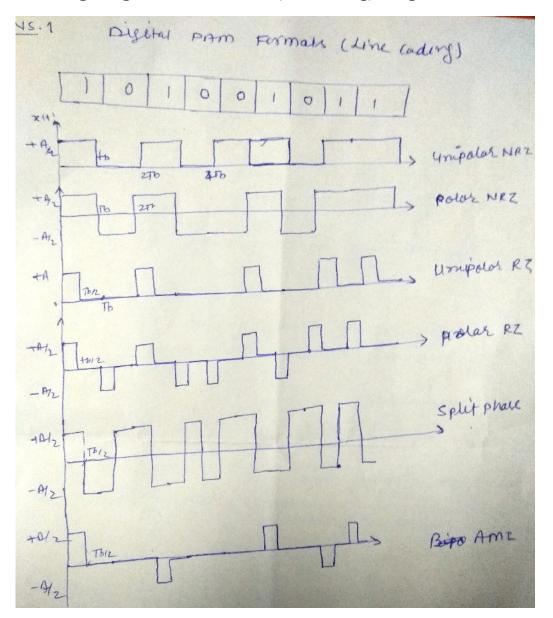
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# JNIT JAGANNATH GUPTA INSTITUTE OF ENGINEERING & TECHNOLOGY JAIPUR I-Mid Term Examination Session 2017-2018 B.Tech III Year VI Semester Branch: ECE Subject: DC

Time: 02:00-03:30 Date: 15-02-18 Subject: DC Subject Code: 6EC4A Max. Marks: 20

Attempt any four questions out of following five questions

# Q.1 Design Digital PAM formats (line coding) for given data.



# Q.2 Explain Base-Band and pass-Band transmission in details.

**Ans.** Communication systems can be classified into two groups depending on the range of frequencies they use to transmit information. These communication systems are classified into BASEBAND or PASSBAND system.

Baseband transmission sends the information signal as it is without modulation (without frequency shifting) while passband transmission shifts the signal to be transmitted in frequency to a higher frequency and then transmits it, where at the receiver the signal is shifted back to its original frequency. Almost all sources of information generate baseband signals.

Baseband signals are those that have frequencies relatively close to zero such as the human voice (20 Hz - 5 kHz) and the video signal from a TV camera (0 Hz - 5.5 MHz). The telephone system used for homes and offices, for example, may transmit the baseband audio signal as it is when the call is local (from your home to your neighbor's home). However, when the telephone call is a long-distance call that is transmitted via microwave or satellite links, the baseband audio signal becomes unsuitable for transmission and the communication system becomes a passband system.

Similarly, transmitting the video signal from your camera to your TV using a wire represents a baseband communication while transmitting that video signal via satellites passband transmission. Therefore, baseband transmission, which is easier than passband transmission, is usually used when communicating over wires, while over-the-air transmission requires passband transmission. Notice that even over wires, the transmission may be passband transmission in specific applications.

Baseband signals are transmitted without modulation, that is, without any shift in the range of frequencies of the signal, and are low frequency - contained within the "base" band of frequencies from close to 0 hertz up to a higher cut-off frequency or maximum bandwidth.

Baseband can be synonymous with lowpass or non-modulated, and is differentiated from passband, bandpass, carrier-modulated, intermediate frequency, or radio frequency (RF).

A passband is in contrast to baseband, whatsoever the range of frequencies or wavelengths can "pass" through a filter. For example, a radio receiver contains a bandpass filter to select the frequency of the desired radio signal out of all the radio waves by its antenna. Hence the passband of a receiver is the range of frequencies it can receive. Q.3 A DMS emits 4 messages with probabilities 1/2, 1/4, 1/8, 1/8 respectively find following parameter.

(a) Total amount of information (b) Entropy

(c)Information Rate d) Efficiency by Using Shannon fano code

x	$P(x_i)$	Step 1	Step 2	Step 3	Code
x <sub>1</sub>	1/2	0		-	0
x2	1/4	1	0		10 119
x <sub>3</sub>	1/8	.1	1	0	111
x4	1/8	1	1	1	111

 $I(x_1) = -\log_2 \frac{1}{2} = 1 = n_1$ 

$$I(x_2) = -\log_2 \frac{1}{4} = 2 n_2$$
$$I(x_3) = -\log_2 \frac{1}{8} = 3 = n_3$$
$$I(x_4) = -\log_2 \frac{1}{8} = 3 = n_4$$

 $H(X) = \sum_{i=1}^{4} P(x_i) I(x_i)$ 

We know that,

$$H(X) = \frac{1}{2}(1) + \frac{1}{4}(2) + \frac{1}{8}(3) + \frac{1}{8}(3) = 1.75$$

or

$$L = \sum_{i=1}^{4} P(x_i) n_i = \frac{1}{2}(1) + \frac{1}{4}(2) + \frac{1}{8}(3) + \frac{1}{8}(3) = 1.75$$
$$\eta = \frac{H(X)}{L} = 1 = 100\% \quad \text{Ans.}$$

Also

# Q.4 A DMS generates 5 messages with probabilities 0.4,0.19,0.16,0.15,0.1 respectively. Find Entropy and efficiency by using HUFFMAN coding.

#### ANS

Solution: The Shannon-Fano code is constructed as follows (see Table 9.12)

$$H(X) = \sum_{i=1}^{5} P(x_i)n_i = 0.4(1) + 0.19(2) + 0.16(2) + 0.15(3) + 0.1(3) = 2.25$$

Also,

 $\eta = \frac{H(X)}{L} = \frac{2.15}{2.25} = 0.956 = 9.5.6\%$  Ans.

4	$P(x_i)$	Step 1	Step 2	Step 3	Code
·1	0.4	0	0		00
r <sub>2</sub>	0.19	0	1		01
	0.16	1	0	No.	10
4	0.15	1	1	0	. 110
r <sub>5</sub>	0.1	1	1	1	111

Table 9.12.

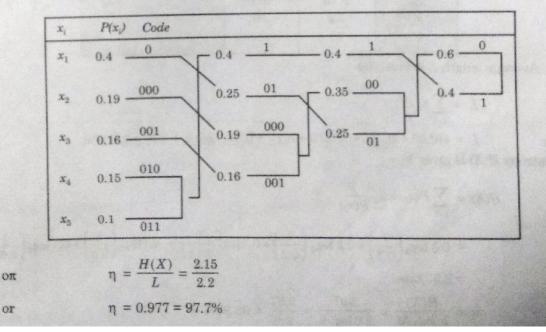
(ii) The Huffman code is constructed as follows (see Table 9.13):

$$L = \sum_{i=1}^{5} P(x_i)n_i$$
  

$$L = 0.4(1) + (0.19 + 0.16 + 0.15 + 0.1)(3) = 2.2$$
 Ans.

or

Table 9.13.



# Q.5 write short notes on;

**A) ISI;-** Unlike analog signals, which are usually smooth in nature, digital signals are composed of pulses with often vertical transitions. The fact that digital signals sometimes have vertical transitions increases their bandwidth significantly since it requires infinite bandwidth to represent a signal with vertical transitions.

Compare for example the bandwidth of two baseband signals given by a sine wave with frequency 0f and a square wave with frequency 0f. The sine wave has a single frequency component at 0f Hz. However, the square wave has infinite frequency components at 0f and integer multiples of it. If we consider the bandwidth of a signal to be the minimum frequency that encloses all frequency components of the signal (the signal has no frequency components at all above that frequency), then the sine wave will have a bandwidth of 0f Hz because it has no frequency components above that frequency, while the square wave has an infinite bandwidth because it theoretically has frequency components that extend to infinity.

The fact that any communication system has limited bandwidth to transmit digital data indicates that certainly a transmitted square pulse will be received differently at the receiver as the channel will filter some components of it. The difference depends on how narrow the bandwidth of the channel compared to the symbol rate in the signal. The effect of filtering part of the transmitted signal by the channel on the quality of the received signal may be significant that a phenomenon called "Intersymbol Interference (ISI)" occurs.

# B) Channel capacity;-

How much data will a channel/medium carry in one second or what is the data rate supported by the channel? Any discussion about the design of a communication system will be incomplete without mentioning Shannon's Theorem. Shannon's information theory tells us the amount of information a channel can carry. In other words it specifies the capacity of the channel. The theorem can be stated in simple terms as follows

- A given communication system has a maximum rate of information C known as the channel capacity
- If the transmission information rate R is less than C, then the data transmission in the presence of noise can be made to happen with arbitrarily small error probabilities by using intelligent coding techniques
- To get lower error probabilities, the encoder has to work on longer blocks of signal data. This entails longer delays and higher computational requirements.

Shannon – Hartley Equation

Shannon-Hartley equation relates the maximum capacity (transmission bit rate) that can be achieved over a given channel with certain noise characteristics and bandwidth. For an AWGN the maximum capacity is given by)

$$C=Blog2(1+SN)\rightarrow(1)C=Blog2(1+SN)\rightarrow(1)$$

Here (C) is the maximum capacity of the channel in bits/second otherwise called Shannon's capacity limit for the given channel, (B) is the bandwidth of the channel in Hertz, (S) is the signal power in Watts and (N) is the noise power, also in Watts. The ratio (S/N) is called Signal to Noise Ratio (SNR). It can be ascertained that the maximum rate at which we can transmit the information without any error, is limited by the bandwidth, the signal level, and the noise level. It tells how many bits can be transmitted per second without errors over a channel of bandwidth (B \; Hz), when the signal power is limited to (S \; Watts) and is exposed to Gaussian White (uncorrelated) Noise ((N \; Watts)) of additive nature.

# JAGANNATH GUPTA INSTITUTE OF ENGINEERING & TECHNOLOGY **JAIPUR**

I-Mid Term Examination Session 2016-2017 **B.Tech 3 Year VI- Semester** 

**Branch: ECE** Time: 2.00pm -3.30pm Date: 14-02-18

Subject: MP Subject Code: 6EC2A Max. Marks: 20

**JNIT** 

Note: Attempt any four questions out of five questions.

#### O.1 How many flag in MP 8085. Explain ?

Flags

The ALU includes five flip-flops, which are set or reset after an operation according to the data conditions of the result in the accumulator and other registers. They are called zero (Z), carry (CY), sign (S), parity (P) and auxiliary carry (AC) flags; their bit positions in the flag register are shown in Figure 3.6. The microprocessor uses these flags to set and test data conditions. For

example, after an addition of two numbers, if the sum in the accumulator is larger than 8-bits,  $G_{12}$  (CY)—to set to one. When an arity chample, after an addition of two numbers, if the sum in the accumulator is larger than 8-bits, the flip-flop indicates a carry—called the carry flag (CY)—to set to one. When an arithmetic operation results in zero, the flip-flop called the *zero (Z) flag* is set to one. Figure 3.6 shows this 8-bit flag register, adjacent to the accumulator.

conclusion of the result is positive, then the displayed providing the tensitient of

F	igure 3.6	shows the	s 8-bit fia	g region	D <sub>2</sub>	D <sub>1</sub>	Do	
	D7	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub> D	P	x	CY	
	S	Z	x	AC A		and the second	-	

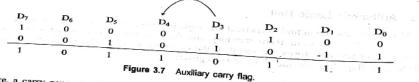
X = Not specified Figure 3.6 Format of the flag register.

The flags are stored in the 8-bit register so that the programmer can examine these flags (data conditions) by accessing the register through an instruction. These flags have critical importance in the decision-making process of the microprocessor. The conditions (set or reset) of the flags are tested through the software instructions. For instance, the instruction JC (jump on carry) is implemented to change the sequence of a program when CY flag is set. The thorough understanding of flag is essential in writing assembly language programs.

Z (Zero) flag: This flag indicates whether the result of a mathematical or logical operation is zero or not. If the result of the current operation is zero, then this flag will be set, otherwise reset.

CY (Carry) flag: This flag indicates whether, during an addition or subtraction operation. carry or borrow is generated or not, if generated then this flag bit will be set. (This flag may also be set before a mathematical operation as an extra operand to certain instructions).

AC (Auxiliary carry) flag: It shows carry propagation from  $D_3$  position to  $D_4$  position. To

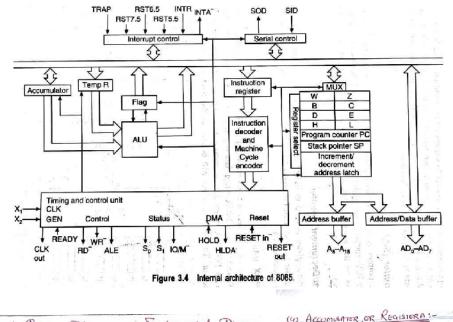


Here, a carry generates from  $D_3$  bit position and propagates to the  $D_4$  position. This carry alled *auxiliary carry*. This flag is never used for provident to the  $D_4$  position. Here, a carry generates from  $D_3$  on position and propagates to the  $D_4$  position is called *auxiliary carry*. This flag is never used for setting or testing a condition. S (Sign) flag: Sign flag indicates whether the result of a mathematical operation is negative or positive. If the result is positive, then this flag will

(bign) hag: Sign hag indicates whether the result of a mathematical operation is negative. If the result is positive, then this flag will reset and if the result is negative this flag ill be set. This bit, in fact, is a replica of the Decking will be set. This bit, in fact, is a replica of the  $D_7$  bit. **P** (Parity) flag: This flag indicates whether the current result is of even parity (1) or of odd parity (0).

and show have the source for

Q.2 Draw and Explain the block diagram of microprocessor 8085. ANS:-



	(4) ACCUMULATOR, OR REGISTORA:-
- Internal Block Diagram or Furdamental Diagram	Stisa point register
- Or Architecture of TNTEL up IC 8085/ 8085A=	- which consists of 8 flip flops so accumulator can store -
- Ab	max 2-bit number.
- BOBS is a 40 pin N-mos tamily IC Consisting of 6200	- The improtance of accumulator is that in most of the
- transistors having power suprly range Vcc=OVthe different	- Orthinatic & Regical operation, up will always take first
- wants this having power outrig raine to some same	- 8-bit number from accumobility, esp will perform the ope-
- parts one described below:-	- retirent in ALO & BISB'S of the result obtained in Alu
	is stored back in accumulator.
- 1) Appress Pins:-	Is store ever at escentester
97 Consists of 16 address pins A15-A8	(5) Temparany Register Wixiz :-
- and ADA- ADO. For setecting one memory location expinil	(5) Lampascuy Register WX72.
- transfer 16: bit address through Abese 16 address fine . 8 ms B's	which store nex b-bit number each-mut write.
- One pransferred - Honorsh 8 upper address pins Ar-As & BLSR'S	compet be used by the programmer.
- are promilered through B-lower adaptes pins Aby-Ano. 0.9.	These registers are used only by up for
- I up will prancher libit number 00004 on actress	: Storing any intermediate data or result of any inter-
- Pins then the very first memory forcation is selected.	hal operation. 25/07/98
	asj <i>01/18</i>
- 27 DATA PINS:-	6 Aw (Avitnematic & logic writ):-
up Bobs has B data Pins Apy-ADO So Apz-	The ALU in up 5085
- Apo king are common unich and had be I	13 of 0 mits 30 rep 2005 13 called 8-bit 2.6.
- ADD EINS are Common which are weed to I make as all	is of a bits so it dos't is caped to bit e.p. The different aminatic & logical operations is berformed
- Apo ting are common which are wred to honster Biss's	The different arthingatic & logical operations is ber formed
- Apo tills are common which are weed to pointer Bisa's - at address as well as 8-bit data but address and - data are prospered at different in	The different arthingatic & logical operations is ber formed
- Apo size are common which are weed to pansfer Bisa's - at address as well as 8-bit data but address and - data are providered at different time. Hence Apo_Apo_ - pine are also called time shared for a line Apr-Apo_	The different appipatic & logical operations is becomed by up in an up 8085 can be trans actionatic & logical operation of max & bit number at a time.
- Apo ting are common which are wred to honster Biss's	The different arthingatic & logical operations is ber formed
- Apo they are common which are weed to honster Bisa's - at address as well as 8-bit data but address and - data are providened at different time. Hence App-Apo - plane are also called time shared for or fime multi- - plexed advess data pine.	The different appropriate & logical operations is becommand by up in an ich 2025 can perform architecting classical operation of max a bit number at a time. 72 Special purpose Registers:
- ADD Star are Common which are weed to honster Bisa's - at address as well as 8-bit data but address and - data are providened at different time. Hence Aoz-ADD - pine are also called time shared for or dime multi- - plexed advess data pins. - (3) General Pureose REGISTERS:-	The different appropriate & logical operatings is berformed by up in an ich 2025 can perform architectic & logical operating of max a bit number at a time. 72 Special purpose Registers:- Caupled ore indeen the til 2001 Space peopler) + pc( traggers)
- ADD Elles are Common which are weed to hansles Bisa's - at address as well as 8-bit data but address and - data are providened at different time. Hence ADJ-ADD - plana are providend time shored for or dime multi- - plexed adress data pins. - (3) GEHERA PURPOSE REGISTERS:-	The different appropriate & logical operatings is berformed by up in an ich 2025 can perform architectic & logical operating of max a bit number at a time. 72 Special purpose Registers:- Caupled ore indeen the til 2001 Space peopler) + pc( traggers)
- ADD Star are Commend which are weed to honster Bisa's - at address as well as 8-bit data but address and - data are prostered at different time. Hence Aog ADD - plane also called time shared for or dime multi- - plexed advess data pins. - (3) General Purpose REGISTERS:-	The different aphipopatic & logical operatings is terformed by up in an ich 2025 can perstrin architectic & logical operation of max a bit number of a time. 3 Special purpose Registers: Special p
- ADD Star are Commend which are used to honster Bisa's - at address as well as 8-bit data but address and - data are prostered at different time. Hence Aog ADD - plane also Called time Shared for or dime multi- - plexed address data pins. - (3) General Purpose REGISTERS:- - Bible each Bici P. E. Hill - Each register Consists of P cion	The different appropriate & logical operatings is berformed by up in an ich 2025 can perform architectic & logical operating of max a bit number at a time. 72 Special purpose Registers:- Caupled ore indeen the til 2001 Space peopler) + pc( traggers)
- ADD Staz are Comment which are used to hansler Bisa's - at address as well as 8-bit data but address and - data are prostered at different time. Hence Aozahoo - pine are also called time shared for or dime multi- - plexed adress data bins. - (3) General Puerose REGISTERS:- - ab Bobs- has 6 registers of - Bobik each Bici D.E. Hill Each register Consists of R FLG.	The different aphippatic & logical operatings is texternal by up in an ich 2005 can perturn artiges is texternal operating of max a tit number at a time. 72 Special purpose Registers: Caused one sinteen up til segister unich consists of 16 Pfe <sup>5</sup> So SP + PC can share max 16 bit number at a time. B) Flag Register :-
- ADD Staz are Commend which are used to hansler Bisa's - at address as well as 8-bit data but address and - data are providented at different time. Hence Aoz-ADD - plane are also called time shared for or dime multi- - plexed advess data bins. - (3) Generes Puerose REGISTERS:- - also Bobs- has 6 registers of - shik each Brich P. E. H Each register consists of R FIGU - So Cash register con store maximum artit on number. - For storing number greater than 8 bits in the	The different appipatic & logical operating is texternal by up in ere set 8085 can perstrin architect & logical operation of max & bit number at a time. 72 Special purpose Resistons: SPC shack panler) + pc( tragson Causici) are tister lips bit acgive which consists of 16 Fless 50 SP + pc can share max 16 bit number at a time. B) Flag Register -
- ADD Staz are Commend which are used to hansler Bisa's - at address as well as 8-bit data but address and - data are providented at different time. Hence Aoz-ADD - plane are also called time shared for or dime multi- - plexed advess data bins. - (3) Generes Puerose REGISTERS:- - also Bobs- has 6 registers of - shik each Brich P. E. H Each register consists of R FIGU - So Cash register con store maximum artit on number. - For storing number greater than 8 bits in the	The different appipatic & logical operatings is terformat by up in an up to be bass can perstrin architectic & logical operation of max a bit number of a time. 72 Special purpose Registers: Second purpose Registers: Sauce panler) + pc( tagson Caunici) are tixleen lies til scripte entite consists of the fle's So sp + pc can share max hobit number at a time. B) Flag Register: S 2 X Ac X P X CF
- ADD Star are Commend which are used to honster Bisa's - at address as well as 8-bit data but address and - data are prostered at different time. Hence Aog ADD - plane also Called time Shared for or dime multi- - plexed address data pins. - (3) General Purpose REGISTERS:- - Bible each Bici P. E. Hill - Each register Consists of P cion	The different aphippatic & logical operatings is terformat by up in ere set 8085 can perstrin architect & logical operation of max & bit number at a time. 72 Special purpose Resistons: Special purpose Resistons: Special purpose Resistons: So special purpose Resistons: Special purpose R

#### Q.3 Explain the function of general purpose register, program counter and accumulator in the architecture of MP 8085.

ANS:-

# 3.4.1 Register Unit

As shown in Figure 3.3, the register unit consists of six general purpose data registers B, C, D, As shown in Figure 5.5, the register unit of address registers PC and SP, one E, H and L, two internal registers W and Z, two 16-bit address registers PC and SP, one increment/decrement counter register and one MUX/DEMUX.

Accumulator A(8)	Flag register	11 langia ushe
B(8)	The contract $C_{(8)}$ and $c_{(8)}$	dayang aslu Ac
D <sub>(8)</sub>	E <sub>(8)</sub>	10112000
. H <sub>(8)</sub>	L <sub>(8)</sub>	acadi or dobib inun cum qun a
Stack poin	ter (SP) <sub>16</sub>	noitestatoin a
Program cou	inter (PC) <sub>16</sub>	particulty character

Figure 3.3 Registers of 8085. It starts Mithal same same status information: HALT, WRITE, READ, 157(5)

## Second of the last General purpose data register

The 8085/8080A has six general purpose registers to store 8-bit data; these are identified as B. C, D, E, H, and L as shown in Figure 3.4. They can be combined as register pairs BC, DE and HI to perform some 16 hit and HL—to perform some 16-bit operations. The programmer can use these registers to store or copy data into the registers by using data copy instructions.

The two internal registers  $\hat{W}$  and Z are also data registers, but these registers are not lable to the user. Micropropriate  $\hat{W}$  and Z are also data registers, but these registers are not XCHG available to the user. Microprocessor uses these registers internally in case of CALL and XCHG

## 30 · maroprocess. ----Program counter (PC)

This 16-bit register deals with sequencing the execution of instructions. This register is a This 16-bit register deals with sequencing bit addresses which is why this is a 16-bit register memory pointer. Memory locations have 16-bit addresses which is the instructions for The microprocessor uses this register to sequence the execution of the instructions. The function of the program counter is to point to the memory address from which the next byte is to be fetched. When a byte (machine code) is being fetched, the program counter is incremented by one to point to the next memory location.

how and a second

#### (4) ACCUMULATOR OR REGISTORA:-

10	Of is a 8-bit register
9	which emisists of & Flip Flops so accumulator can store -
and the	max & bit number.
	The importance of accumulator is that in most of the
	arthimatic & logical operation, up will always take fint
	8-bit number from accumolator, sup will pertorm the ope-
	ration in ALU & BLIB'S of the result obtained in ALU
	is stored back in accumulator.

#### Q.4 Explain addressing modes of microprocessor 8085 with examples.

	1
Addressing Martes of isp Bobs 1-	
For performing a	in Promotion in the time to a promote Prestion
and the interview of the state of the state of the state	my for executing the instruction is begent in memory existion
operation using up, we have to give me course	me. and to bit address of this memory location is given along
ing instruction to eat. In each instruction, weh	ave with the instruction. Such instructions are as rated DAMA.
to give three information	inspection . R.g.
(i) maryation to be perform	- Dood M
(2) Advess of source of date which is securing	16 trait guar
for performed of "operation	Adds: TI
(2) Address of distingtion of result conico is obtain	pd
. (3) Hald 25 & d- Construction 1/ construction	BEH Momoy
after the operation allow I so wall	4
The method by contin coldness of source of do	(1) Register Indirect or Indirect addressing mode (RIAM):-
or Address of destination of result is given in the	
- instruction is called as addressing mode.	\$116 bit data required for executing the instruction is
- These are five types of addressing moder in	present in memory Poration, the actives of this memory
10 p B0851	location is present in register bais and the 20 hame of this
D Immediate addressing mode (IAM) :-	Concertion is provent in seguriter para and the solution
9F 8 1651-	register pair is given with the instruction such instruction are
a data serviced for and executing the instruction	called RIAM instruction.
- is swan directly along with the influction then such	C-9. B - B - 00004
- instructions and called immediate addressing ouch instru-	LDAX B > 34 OT BOUCH
- instructions and salver instructions, o the last alphase	16 - 751 guora
	Addrews I I
- 15 T. 21.	Va - ALEEM
- MNI A.75H	[751] MEMORY
	1.08
- (2) Regista direct or Registor addressing mode: - (RDAM,	2
94 S/10	6F-
- data required for executive instruction is present in	(B) Implicit cultonessing mode (IMM):-
- B/16 bit register/ Resisterfair and the name of this segiste	st address of source
( The register pair is given along with the instruction,	of data as well as address of destination of result is
I such instruction are called register direct addressing made	Fired, they there is no need to give any oprend along
- inchaction Mov AB	with the instruction. such instructions are called implicit
四日 日子 四日	a hand the mather soon inspections end called implicit
- (8) Direct addressing mode (DAM) :-	_ addressing mode instruction. or Inherent addressing mode
- 3	instruction e.e. CMA
	- RAR

Q.5 Explain the instructions MOV A, M, SHLD A000 H, LDA DADA H with addressing Mode flag effect and machine cycle.

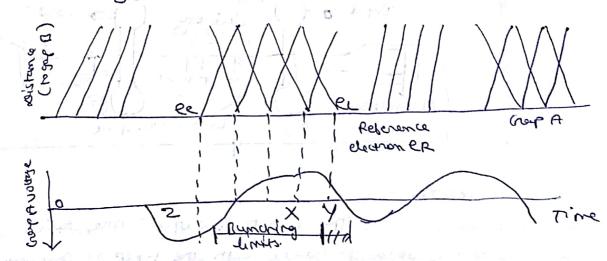
	1	G	c . ]	1 1		6000H
		10		,6		
4> Mor Rd, M L Move data from scheded memory location		·	754 10	0		1
(FR) to destination register Rd]		D	6		754	20004
memory <u>Addressing mode-S -&gt; [RIAM]</u> , [SB]		20	00 -	Address () But		
(ALT X ATX d > [RDAM], [NFAC]		H	1	But		
HIL B RA						t sure t
MOY AM			1		heh	I ffsfm
MON B, M			up sour			1
may C. M	e.9 Tr	anster	bibit n	a of menas	my loc.	tion ffffy into Acc.
MON DIM	801 -		H, FFF	FH		<u>.</u>
	80 <sup>4</sup> -	LXI	H, FFF	Рн		
MON DIM	80 <u>1</u> -	MON	A, M			
MON DIM MON E.M MON HIM MON LIM	801-	MON	A, M		0000×	* *
MOV DIM MOV E, M MOV HIM MOV LIM	<u> </u>	MON	A, M		-H1000	
MOV DIM MOV E, M MOV HIM	<u> </u>	Mox	A, M		-H1000	
Mov BIM Mov E. M Mov HIM Mov LIM 20001 2.1 transfer 2-bit data of memory focation into register c.	<u> </u>	MON	A, M		-H1000	

useloof to	
13) SHLD Add - 46 ( store 4.2 pair direct into two memory (FRR WH) (Braching more address is sized internation	(FRR) (16), it) if load accomutator from memory data (FRR) (100; address is given in the instruction)
L X IS HUNDER H X IS HUNDER S-> [RDAM], [TBI] [NFAR]	Addi X & XX & ARDAN] (TBI), [NFAC]
Q3. (1) SHLD 4100H	eg. Transfer schit no. of womany concertion 4000 H into acc. by four different methodic.
C.A. D Stopp 16 bit no of the Dire into two menory long. Sace 22044	Nov AIM
MOY H, D EXCHG	
SHLD 9000H	when a start of the start of th

Sybject - MW-II DATE: 1 PAGE NO. : out if notherage & winatic & mechanics & operation of two of <u>g</u> Cavity Klystron ? In two Cavity Klystron, high velocity electron beam i P formed, focused & sent down along a glass tube to a collector electrode, which is at high positive patential with respect to cathode. Buncher avit Catcher Couring Erfut a 3 OUTPUT electron bunches colector (a)debartel Troused on space (4) Operation -. The input & output are stallen from tube via sevenant lawing with the help of Gupling Joops. The region bet" buncher lawity & latcher lawity is called drift sparce. The first electrode controls the No. of electrons in the electron beam & serves to focus the beam. The velocity of electron . in the beam is determined by the beam acclerating potential. on lawing the finegion of focusing grid, the electron passer through grids of buncher Cauity - The space beth The grids is referred to as intersection space. When electron Travel through this spale, they are subject to RE potential at frequency determined by Cavity Rest frequency which is wathing but The input prequency. **Teacher's Signature** 副連邦 起朝局 ウカーシードの

Velocity Moduleston ... Consider a situation where there is NO Velocity Moduleston ... Consider a situation where there is NO Velocge almoss the gap. Electrony passing through gap if are imableted & continue on to the celector with same constant velocity they had before opproaching gap A. When RF signal to be amplified is used for esciciting the buncher Country thereby devolping an alternative voltage of signal frequency allows gap A.

At point X on input RF Lycle, alternating No wage is o & electron win parses through gap A is malleded by RF Signel. set this electron is called reference electron ex which travels to with an unchanged velocity No = Jain V is anode to cothode bactoge.



So, when electrons pars es the buncher gap, their velocity will have changed accordance to the input RF signel.

Jet veraus the basic basic of homen's of Helix tube twit tube & explain its operation.

See The TWIT is a high gain, low weise I wide band width amplified which can operate a wide range of frequencies from Iw MHZ-JOWH. TWIT is also known as stelig Travelling wave true. The TWITA is an amplifier which make use of disturbed interaction bet an electron beam & travelling wave RIF field. To make dure, the interaction wet an electron from & a RF Field, it is releasing

DATT: 1 1 MORNO.: 2 to ensure that they both are travelling in the on me direction with dame velocity. It differs from Klystron complication in which electron beam travel but RF field remained attactionary. RF. OLP Actendent V RFIC 6.5:1.5 (allector electron Helix electron gun deam wave line operation - In, Twit, process state place continuity over entire length of alow wave structure. The applied signal propagate around turns of helix Eigenduces an electric field along ares of helix which progress along a rial direction with phose lieboing which is aroall compared to velocity of light. This axial time varying electric field produces vers it modulation in an otherwise uniform velocity which is small compared to votocity of ly equal to phase velocity of electrons in electrons beam nowing through nelix axis. The velocity modulation tends to bunch the electrone i when a signal voltage is coupled into helix. axial electric field exerts a force on electron of Retarding F= - eE Devese in electron Travelling electronog renz density field e 0 Bunch elictron begin According for o consider point A, electrons aread as it are nowing more dower than average & those behind them the around Trachar's Signature

point A. Since, de electron velocity is slightly greater than the axial wave velocity, it result into a dituation in which more electron face the retarding field than the according field; do energy in thus last by the electron beam & gained by the travelling wave. resulting in an amplified signal. At next turn as helix, RFSignel amplitude is more and also the electric field axis created by The RFSignal is more. Hence, force due to electric field is more & bunching take flace.

The electrons enter gap at Z = 0.  $V = \int \frac{de_{10}}{m}$ 

$$(f) = \int_{\Phi} \frac{1}{2} \int_{\Phi} \frac$$

Now, voltage at Point A= U= Vo + Visinw t

doctage signerance, 
$$-VR - (VO + Visinwit) = -VR - VV$$
  
 $E = (- VR - VO)$ 

force on electron, 
$$= -eE = e\left(-\underline{vR}-\underline{vo}\right) = e\left(\underline{vR}+\underline{vo}\right)$$

111 2 - 11 PAGE NO. : NOW, equating eq. 4 h eq. 3, md22 - e (VR+10) d+2 L 222 <u>e (VR+VO)</u> 5 Integrating, d2 = e (UR+V) J+C d+ mL 0  $t=t_1$ ,  $d^2 = V_1$ VI = C (UR+UD)JI+C C= VI-C (VR+VO) JI Substituty value of a from ()  $\frac{d2}{dt} = \frac{e(v_{R+V_0}) \pm + v_{I} - e(v_{R+V_0}) \pm t_{I}}{m_{L}}$ d2 = e (vr+ Vo) (J++) + VI (8) Integrating,  $Z = \mathcal{L} (VR + VO)(t - t_i)^2 + V_i t + (\overline{O})$ 2mL $0 = \frac{e}{2mL} \left( \frac{\sqrt{2}}{2mL} - \frac{1}{2mL} \right) \left( \frac{1}{2mL} - \frac{1}{2mL} \right)^{2} + \frac{1}{2mL} \left( \frac{1}{2mL} - \frac{1}{2mL} \right)^{2}$  $H_{2=0, t=t_{2}}$  $\frac{C_1 = -e \left( UR + UO \right) \left( \pm 2 - \pm 1 \right)^2 - V_1 \pm 2}{m_2}$ Substituting value  $d_{C1} = \frac{1}{2} \cdot \frac{1}{2$ Again, When t= t1, Z=0 **Teacher's Signature** 

$$\frac{-e^{\alpha}}{2\pi} (v_{R}+v_{0}) (z_{2}-z_{1})^{2} - v_{1} (z_{1}-z_{2})_{z_{0}} (v_{1}-z_{2})_{z_{0}} (z_{1}-z$$

94

DATE: 1 1 PAGEHO.: Y AT X'= 0.734, Y'JI(X') = 0.253 JI(Y')= 0:345 output power Pac = 40x 20x103x 1x0345 lac = 0.276W  $\frac{1}{2} \frac{1}{2} \frac{1}$ 05 A helix WT, openates at 46HZ under a learn voltage of 10 ICU & beam current Sw mA. St hell'x inped ence is 25 or & length is 20 cm, find old Power gamin do? Sal 6= 46HZ, VO= loKV, TO=SWMA 20= 25s, l= 20cm. output gain = Ap= - 9.54 + 47.2 NC da. N = 1Be = QT = W = Ae = QTVO  $Ae Vo \qquad W$   $Vo = J2eVo = 0.593 \times 10^6 \text{ Jvo}$ No= 0.593× 10° mls. & W=200  $N = 102 - 0.2 \times 2T \times 4 \times 10^{2} = 13.49$   $3\pi v_{0} = 8\pi v_{0} \times 593 \times 10^{8}$ Coupling factor Cis C= (Io20)112 4Vin  $C = \left(\frac{500 \times 10^{-3} \times 25}{4 \times 10^{-3} \times 10^{-3}}\right)^{1/3}$ Teacher's Signature



C= 0.068

olp lower gain AP is

Far week a site in set of a site of

1 14 6 2 2 2

and the second a start in

1 21 × 1 1 × 20 - 6 - 6

AP = -9.54 + 47.3 NC $= -9.54 + 47.3 \times [3.49 \times 0.069$ 

= 3 ].82 gB

Prover and the State of the second state

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- OV

1. 1 23 3